Reviewing SPICE Threshold-Voltage and Threshold-Current Memristor Models and Applications

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Abstract—The technology scaling is achieving the physical limits of transistor dimensions. New devices are been investigated in recent years. The memristor is one of the most promising ones. This paper presents a review of memristors models reported in the literature. A deep discussion is performed considering two open source SPICE models, each one with different threshold parameter. One is controlled by voltage, and the other controlled by current. Applications of memristive logics — as Memristor Ratioed Logic, Memristor-Aided Logic and IMPLY — were explained, simulated and presented in order to validate the functionality of these models.

Index Terms—memristor, SPICE models, memristive logic, threshold control.

I. Introduction

Since the last years, some well-known walls impaired computer revolution [1]. The memory wall is one of them, in which processors performance grows faster than memories performance throughout the years. Thereby, it implies that a crescent gap between the time required for memory access and processing time became a problem. This circumstance leads to memory access time the main limiting factor in massive data usage applications [2]. Another wall that becoming even bigger today is the power wall. Mainly in High-performance computing (HPC) applications, power consumption brings a limit in how much a processor can dissipate power. In the past, technology could be improved, choosing only performance in a trade-off. However, today, the energy consumption is not forgetful. CMOS scaling has been a solution for many years. Nevertheless, it is facing barriers to development as well. Scaling compromises reliability, reducing lifetime and fault coverage [3]. Another barrier faced by digital designers is leakage (the current that flows in the switching of a device, generating static consumption). As more as a device scales, the greater the leakage problematic tend to be. In some cases, static consumption can be higher than dynamic ones [4].

The scaling issue causes a slowdown in transistors miniaturization, obtaining a harder scenario to achieve the density predicted by Moore [5]. Thereby, the memristor is a suitable candidate to overcome this situation, by complementing or even substitute CMOS. Also, it is the best candidate for memory and neuromorphic [6]. Besides this, there are other observable qualities of memristor, that are: Null static consumption [7], non-volatility, high device density [8]–[11], good scalability [2], high CMOS compatibility [12]–[14] and it can store multiple bits in the same device [15].

Despite high research interest in memristive devices, is not that effortless to use a model without having to disposal a high-cost software. In this work, some models were reviewed, giving special attention to two chosen models which were explained in more depth. Both models were developed in SPICE language and work well in an open source software (as Ngspice, that this work uses), one controlled by voltage [16] and one controlled by current [17]. In section II, a theoretical background is given. An overview of models in the literature is present in Section III. The chosen models are explained with more details in Section IV, and in Section V, applications for memristors are simulated and demonstrated. Finally, in Section VI, the conclusion is shown.

II. Background

Memristors were idealized in 1971 by Leon Chua [15], aiming to fill a gap between electric charge and magnetic flux, because no device relates these two fundamental variables of electronics. With this, a fourth fundamental element was suggested to complement resistor, capacitor, and inductor. Memristor (a contraction of memory resistor) could not be physically implemented, due to limitations of that time. Only 37 years later, in 2008, researchers from Hewlett-Packard have announced what would be the first physical memristor [18]. Since this, a large group of researchers started to invest their knowledge and time to make memristors a reality[12].

What characterizes a memristive behavior is the non-linear function between current and voltage, in addition to that, a memristor can change its resistance. This property is the hysteresis, in which the previous state influences the present state, as an intrinsic memory. This behavior can be observed when a Current (I) versus Voltage (V) graph is plotted, showing a hysteretic curve given by Lissajous figure, which is a complex harmonic motion resulting from a system of parametric equations. Fig. 1 demonstrates the curve made with chosen models.

In practice, a memristor can hold its logical state by its resistance. The resistance can be low (R_{ON}) or high (R_{OFF}), characterizing an "ON" and "OFF" state, respectively. The control of this resistance states is given by the voltage/current
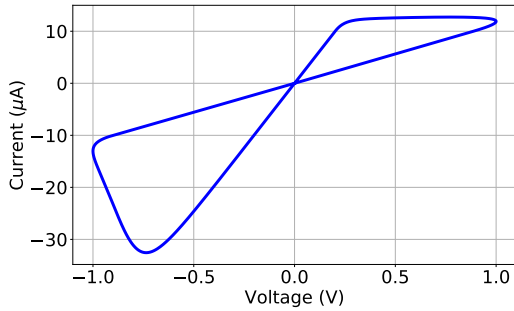
Fig. 1. Histeretic curve plotted from current versus voltage using the memristor model proposed by Dias et al. [17]

flow direction. As shown in Fig. 2, when the voltage/current flow in the positive terminal direction, the resistance of device increases. Otherwise, in the opposite direction, the resistance decreases.
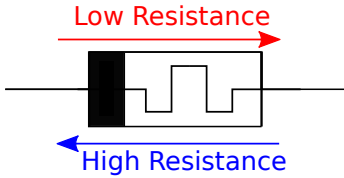

Fig. 2. Memristor state change reference. When the current/voltage come into device, it changes or stay at R_{ON}. When the current/voltage flow out of device, it change or stay at R_{OFF}.

III. MEMRISTOR MODELS OVERVIEW

In this section, the main models proposed in the literature for the memristor simulation are discussed. Biolek et al. [19] proposed a model based in the first memristor announced, made of TiO_2 in HP Labs. The physical memristor was represented by an equivalent circuit, in which two series resistances simulates the physical behavior of the two regions of a real model of TiO_2. Furthermore, the memory is modeled by an integrator controlled by feedback, which stores the effects of the current through the memristor.

Abdalla et al. [20] proposed the Simmons Tunnel Barrier model that uses a resistor in series with an electron tunnel barrier instead of two series resistors. Due to this modification, the behavior of the model is non-linear and has asymmetric state changing, which became closer to reality, because memristive devices are highly non-linear [21]. The main parameter of this model is its tunnel barrier width. Wherein its derivative can be interpreted as the drift speed of oxygen gaps. Several adjustment parameters are used, giving special attention to i_{ON} and i_{OFF} that restrict the threshold currents.

Although realistic, the Simmons model was complicated and had limitations, motivating Kvatinsky et al. [21] develop an improved version, the ThrEshold Adaptive Memristor model (TEAM). The critical factors of this improvement are the explicit relationship between current and voltage and different from the previous one — which could only represent a

single device — the TEAM model allows the possibility of representing any memristive device. This flexibility is given by the expression of the derivative of an internal state.

A compact model from Stanford University aimed at metal-oxide-based bipolar resistive random access memory (RRAM) applications was present in [22]. Unlike previous compact models, this model includes the effects of Joule heating and temperature change. Furthermore, filament growth and rupture physics provide the basis of the model. It reproduces the transient response, the statistical variation, and the exponential voltage–time relation of the memory cell that can be observed in the experiments shown in the proposed work.

Kim et al. from the University of Minnesota (UMN) present the UMN STT MTJ model, an compact SPICE model of an STT-based MTJ which explore virtual current and voltage nodes in the electrical scheme. The model explores the magnetization and effective magnetic field described in several studies. Geometrical sizes and properties of MTJ were also taken into account [23].

In addition to these models, there is the voltage controlled model made by Pershin and Di Ventra [16], which have the threshold voltage parameter, a significant value that can be controlled in a practical and intuitive form. Considering problems in some applications, Dias et al. used the Pershin model as the basis to develop a model with two important modifications [17]: The first one adapts all the parameters expressed as voltage to equivalent parameters based on current. With this, the behavior of the model resembles the STT MTJ, allowing applications such as IMPLY logic, which could not be made with the other model. The second modification is a mathematical remodeling that improves the accuracy of the simulations. The following section explains how the threshold controlled models work.

IV. THRESHOLD MODELS OPERATION

Two models were chosen to a depth explanation in this work. The reason for this choice consists in having a comprehensive threshold parameter and work well in an open source SPICE simulation tool. Ahead, the voltage controlled and the current controlled model will be explained and demonstrated.

A. Threshold voltage model

In [15], equations were demonstrated to describe memristive devices that can be both used to current and voltage control. Pershin and Di Ventra focused on voltage controlling form in their work. A system of equations that was suggested specifically to voltage-controlled systems to represent the memristive behavior, as follows:

$$I = X^{-1} \tag{1}$$

$$\frac{dX}{dt} = f(V_m)[\theta(V_m)\theta(R_{OFF} - X) + \theta(-V_m)\theta(V_m - R_{ON})] \tag{2}$$

In which,

$$f(V_m) = \beta V_M + 0.5(\alpha - \beta) + [|V_M + V_T| - |V_M - V_T|] \tag{3}$$

The mentioned threshold voltage V_T is shown in (3). R_{ON} represents the minimum and R_{OFF} the maximum resistance assumed by memristor, i.e., the limiting values of memristance X. θ stands for step functions which serve to enframe the memristance value between R_{ON} and R_{OFF}. Furthermore, α and β are significant coefficients used to control the slope inclination when memristor change its state. Each value stands for one memristance change, α when $|V_M|$ (memristor voltage) is greater than V_T, and β when $|V_M| < V_T$.

An equivalent subcircuit schematic is proposed to simulate the model. A behavioral resistor receives the absolute value of memristance, represented by the X of (2). This value is given by the voltage in a wire between a current source and a capacitor. The two terminals of the model are the same as the behavioral resistor. A SPICE code was described for Ngspice circuit simulator is present in Table I.

The second line on the code is a behavioral source. In other words, a non-linear dependent source, in which control the current through ternary functions looking forward to maintaining memristance between R_{ON} and R_{OFF}. The third line of Table I is the capacitor declaration, and the "Rmem" line states the behavioral resistor that receives the valor of voltage in X of the wire between the source and capacitor, as informed before. The penultimate line (before subcircuit ends) provides the implementation of (3).

TABLE I
VOLTAGE THRESHOLD MODEL DESCRIPTION

```
.subckt memristor plus minus PARAMS: Ron Roff Rinit alpha beta Vt
Bx 0 x I='((f1(V(plus)-V(minus))> 0) && (V(x) < Roff)) ? f1(V(plus)-V(minus)):
  ((((f1(V(plus)-V(minus)) < 0) && (V(x)>Ron)) ? f1(V(plus)-V(minus)): 0)) '
Cx x 0 1 IC=Rinit
Rmem plus minus r=V(x)
.func f1(y)=beta*y+0.5*(alpha-beta)*(abs(y+Vt)-abs(y-Vt))
.ends
```

B. Threshold current model

Posteriorly, the Pershin and Di Ventra model served as a basis to a novel current controlled memristor developed by Dias and Butzen [17]. Besides the control based in current, meaningful mathematical and logical implementations were made to enhance the previous model. Dias proposed a new equation system to improve simulation accuracy, wherein a specific behavior operate in each state transition of the device, according to (4):

$$\frac{d(R_{MEM})}{dt} = \begin{cases} f_1(I_{MEM}, R_{MEM}), & I_{MEM} > 0 \text{ and } R_{MEM} < R_{OFF} \\ f_2(I_{MEM}, R_{MEM}), & I_{MEM} < 0 \text{ and } R_{MEM} > R_{OFF} \\ 0, & Otherwise \end{cases}$$

(4)

Functions f_1 and f_2 have a similar structure. However, each one has a different factor of proportionality Kp, that can be differentiated by a general function f_n described as follows:

$$f_n(I_{MEM}, R_{MEM}) = \theta_1 + \theta_2 \cdot \theta_3 \quad (5)$$
$$\theta_1 = Kp_n \beta I_{MEM} \quad (6)$$
$$\theta_2 = 0,5Kp_n(\alpha - \beta) \quad (7)$$
$$\theta_3 = (|I_{MEM} + I_T| - |I_{MEM} - I_T|) \quad (8)$$

The efficacy of mathematical modeling was demonstrated in their work, reaching significant results in percentage convergence error analysis in each type of state transition simulations. Mainly in 80k$\Omega \rightarrow$ 10kΩ transition, an impactful improvement was noticed when compared to the other model. A maximum error below 0.2% was apparent in Dias et al. mathematical modeling, versus 17.42% in Pershin et al. modeling, overcoming the high level of inaccuracy.

V. APPLICATIONS

In order to validate the memristors functionality, three proposed logic implementations were simulated and present. The Memristor Ratioed Logic (MRL) executes AND and OR operators with only two memristors. The inputs are connected in each memristor in the same terminal, and output is given by the voltage in a node connected in the other side of devices at the same time. The only difference between AND and OR logics is the terminal orientation of devices, in which inputs in negative nodes represents the OR logic, otherwise, AND logic. NAND and NOR gates can be implemented with a CMOS hybrid circuit, using CMOS inverter. All simulations used the parameters present in Table II, the simulations using MRL logic is present in Fig. 3.

TABLE II
PARAMETERS DESCRIPTIONS AND VALUES IN SIMULATION

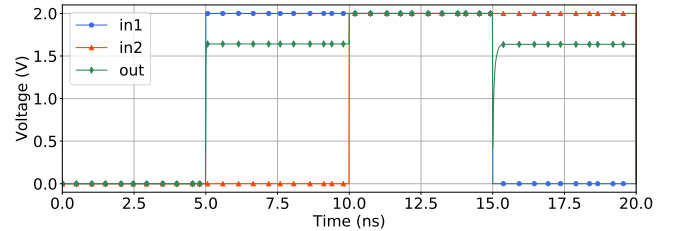| Parameter	Description	Value
R_{ON}	Minimum resistance	$1k\Omega$
R_{OFF}	Maximum resistance	$20k\Omega$
I_T	Threshold current (Dias et al. Model)	$10\mu A$
V_T	Threshold voltage (Pershin et al. Model)	$1V$
α	Memristance growth rate ($|I_M| > I_T$)	0
β	Memristance growth rate ($|I_M| < I_T$)	2×10^{19}
C_1	Compensation parameter	0.25

Fig. 3. MRL OR gate. Sample simulated with Pershin et al. model. Dias et al. present the same behavior.

Another proposed logic is Memristor-Aided Logic (MAGIC). As MRL, it works with both voltage or current controlled device. The main difference of this logic is to validate the logic by the actual resistance of the memristive device, instead of voltage in nodes. The inputs are the initial state of memristors, and the output is the final resistance of a third element. Store the output value at the same time the logic is done allows logic-in-memory applications, as shown in [24]. To exemplify the functionality, NOR gate was implemented in this work using MAGIC logic. The logic

requires some conditions: The output memristor must be in a high state (R_{on}), that is, low resistance. Besides that, a voltage is applied in both input memristor to validate the logic; it needs to be lower than the threshold when both inputs are "0", and higher than the threshold in any other case. This requirement is due to the output memristor starts in logic "1", in which NOR operation only results in this case when both inputs are "0", if any voltage/current becomes higher than the output device threshold, it changes to high resistance. Fig. 4 shows all outputs for all input combinations.
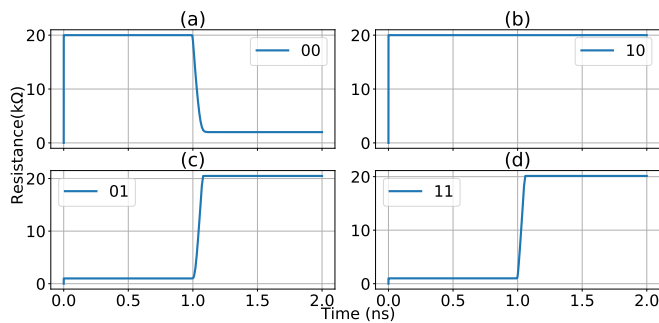

Fig. 4. MAGIC NOR gate. The images show outputs for given inputs labeled in each image, in1, and in2, respectively. The logic is validated after 1ns. (a) shows the unique output resulting in logic "1"(R_{ON}). (b), (c) and (d) present a logic "0"(R_{OFF}) output, for any low resistance input.

Lastly, there is the IMPLY logic, in which it cannot be implemented with voltage controlled memristor. The reason for it is a mandatory set of equations that must be fulfilled. While using the model proposed by Pershin et al. two equations conflict, if one is satisfied, another one cannot be and vice versa. With this, only the current controlled memristor proposed by Dias et al. can be used in this logic application. The logic uses only two memristors, like MAGIC logic, the inputs are the initial state of devices and use resistance as inputs and output. However, in a $P \rightarrow Q$ operation, the result of implication is set on the memristor that represents the variable Q, instead of requiring a third device. A series of implies can be equivalent to any logic; to do this, auxiliar memristors must be used to realize some operations. Simulations were done and shown correct results.

VI. CONCLUSION

The work presents a review of memristive devices of literature, mainly two models were explained with more details. The chosen models exposed in work can be simulated in an open source SPICE simulator, avoiding high-cost tools. Furthermore, simulations were done in order to validate the model's functionality in the given logics. MRL logic presents a high signal degradation, hardening logic with devices in cascade without a signal restoration. Future works aim in memory-in-logic applications.

REFERENCES

[1] D. A. Patterson, "Future of computer architecture," in *Berkeley EECS Annual Research Symposium (BEARS), College of Engineering, UC Berkeley, US*, 2006.

[2] S. Hamdioui, S. Kvatinsky, G. Cauwenberghs, L. Xie, N. Wald, S. Joshi, H. M. Elsayed, H. Corporaal, and K. Bertels, "Memristor for computing: Myth or reality?" in *Proceedings of the Conference on Design, Automation & Test in Europe*. European Design and Automation Association, 2017, pp. 722–731.

[3] EU-Commission *et al.*, "Next generation computing roadmap, a study prepared for the european commission," *European Union*, 2014.

[4] B. Hoefflinger, *Chips 2020: a guide to the future of nanoelectronics*. Springer Science & Business Media, 2012.

[5] G. E. Moore *et al.*, "Cramming more components onto integrated circuits," 1965.

[6] M. e. a. Wang, "Robust memristors based on layered two-dimensional materials," *Nature Electronics*, vol. 1, no. 2, p. 130, 2018.

[7] D. Fan, M. Sharad, and K. Roy, "Design and synthesis of ultralow energy spin-memristor threshold logic," *IEEE Transactions on Nanotechnology*, vol. 13, no. 3, pp. 574–583, 2014.

[8] M.-F. Chang and et al., "Challenges and circuit techniques for energy-efficient on-chip nonvolatile memory using memristive devices," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 5, no. 2, pp. 183–193, 2015.

[9] A. Kawahara *et al.*, "An 8 mb multi-layered cross-point reram macro with 443 mb/s write throughput," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 1, pp. 178–185, 2012.

[10] S. Hamdioui, H. Aziza, and G. C. Sirakoulis, "Memristor based memories: Technology, design and test," in *2014 9th IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS)*. IEEE, 2014, pp. 1–7.

[11] L. Chua, "Resistance switching memories are memristors," *Applied Physics A*, vol. 102, no. 4, pp. 765–783, 2011.

[12] C. de S. Dias, "Aplicação da tecnologia memresistiva ao projeto de sistemas digitais através da exploração de circuitos híbridos e implicação material," Master's thesis, FURG, 2018.

[13] Q. Xia *et al.*, "Memristor- cmos hybrid integrated circuits for reconfigurable logic," *Nano letters*, vol. 9, no. 10, pp. 3640–3645, 2009.

[14] Y. Zhou, Y. Li, L. Xu, S. Zhong, R. Xu, and X. Miao, "A hybrid memristor-cmos xor gate for nonvolatile logic computation," *physica status solidi (a)*, vol. 213, no. 4, pp. 1050–1054, 2016.

[15] L. O. Chua and S. M. Kang, "Memristive devices and systems," *Proceedings of the IEEE*, vol. 64, no. 2, pp. 209–223, 1976.

[16] Y. V. Pershin and M. Di Ventra, "Spice model of memristive devices with threshold," *arXiv preprint arXiv:1204.2600*, 2012.

[17] C. d. S. Dias and P. F. Butzen, "A novel spice model of memristive devices with threshold current based control," in *2018 31st Symposium on Integrated Circuits and Systems Design (SBCCI)*. IEEE, 2018, pp. 1–6.

[18] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *nature*, vol. 453, no. 7191, p. 80, 2008.

[19] Z. Biolek, D. Biolek, and V. Biolkova, "Spice model of memristor with nonlinear dopant drift." *Radioengineering*, vol. 18, no. 2, 2009.

[20] H. Abdalla and M. D. Pickett, "Spice modeling of memristors," in *2011 IEEE International Symposium of Circuits and Systems (ISCAS)*. IEEE, 2011, pp. 1832–1835.

[21] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Team: Threshold adaptive memristor model," *IEEE transactions on circuits and systems I: regular papers*, vol. 60, no. 1, pp. 211–221, 2012.

[22] X. Guan, S. Yu, and H.-S. P. Wong, "A spice compact model of metal oxide resistive switching memory with variations," *IEEE electron device letters*, vol. 33, no. 10, pp. 1405–1407, 2012.

[23] J. Kim, A. Chen, B. Behin-Aein, S. Kumar, J.-P. Wang, and C. H. Kim, "A technology-agnostic mtj spice model with user-defined dimensions for stt-mram scalability studies," in *2015 IEEE custom integrated circuits conference (CICC)*. IEEE, 2015, pp. 1–4.

[24] A. Haj-Ali, R. Ben-Hur, N. Wald, R. Ronen, and S. Kvatinsky, "Not in name alone: A memristive memory processing unit for real in-memory processing," *IEEE Micro*, vol. 38, no. 5, pp. 13–21, 2018.